AMENDMENTS

In the Specification

Please replace the paragraphs 0035-0039 with the following amended paragraphs.

At [0035]:

In process step 1a, trench openings and via openings are etched in dielectric layers previously deposited on a semiconductor wafer. This is carried out by patterning a photoresist layer on each dielectric layer and etching the trenches and vias in the respective layers, as is well-known by those skilled in the art. After the trench and via openings are etched in the dielectric layers, the photoresist is stripped from the layers.

At [0036]:

In process step 2a, the wafer W is placed on the wafer heating apparatus 8 in the pre-clean chamber 1, as shown in Figure 2. In process step 3a, the wafer W is simultaneously subjected to pre-cleaning and degassing. Accordingly, the temperature controller 22 is used to heat the wafer heating apparatus 8 and wafer W to a target processing temperature which is optimum for pre-cleaning of the trench and via sidewalls etched in the dielectric layers on the wafer W. Preferably, the wafer heating apparatus 8 is used to heat the wafer W to a temperature of at least typically about 150 degrees C. Most preferably, the wafer W is heated to a temperature of at least about 350 degrees C.

At [0037]:

After the wafer W is heated to the target processing temperature, hydrogen or ammonia gas 28 is introduced into the chamber 1 through the gas inlet 14. Source RF power of typically about larger than 200 watts is applied to the chamber 1 to ionize the hydrogen or ammonia gas and form a plasma in the chamber 1. A bias RF power of typically about 0-400 watts is applied to the wafer W by the RF bias 26. Accordingly, positive ions formed in the plasma strike the trench and sidewalls on the negatively-charged wafer W, thereby etching chemical residues and oxides from the sidewalls. Also, gases such as water vapor and oxygen are driven from the trench and via sidewalls as those surfaces are degassed at a temperature of typically about 300 degrees C. The pre-cleaning and de-gassing step 3a is continued for a time period of typically about 30-120 minutes to ensure optimum pre-cleaning and degassing of the trench and via sidewalls prior to subsequent deposit of a metal barrier layer on those surfaces.

At [0038]:

In process step 4a of Figure 3, the wafer W is removed from the pre-clean chamber 1. In process step 5a, a metal barrier layer is deposited on the trench and via sidewalls and bottoms. This step usually involves deposition of a Ta or TaN layer on the bottom and sidewalls of the trench and vias using an ionize PVD process, according to the knowledge of those skilled in the art.

At [0039]:

In process step 6a, a metal seed layer, typically copper, is deposited on the metal barrier layer. This step is typically performed using a conventional CVD process. In process step 7a, the trenches and vias are filled with copper, typically using conventional electrochemical deposition (ECD) techniques. Finally, the dual damascene structure is completed by subjecting the copper to CMP (chemical mechanical planarization) to remove copper overburden from the structure.